**PROBLEM STATEMENT: -**

Q1. Design suitable data structures and implement pass1 of a two pass assembler for pseudo-machine.

START 100  
A DS 3  
L1 MOVER AREG, B  
ADD AREG, C  
MOVEM AREG, D  
D EQU A+1  
L2 PRINT D  
ORIGIN L2+1  
MOVEM AREG, ='34'  
MOVEM AREG, ='14'  
LTORG  
STOP  
MOVEM AREG, ='143'  
MOVEM AREG, ='134'  
B DC '19  
C DC '17  
END

Q2. Design suitable data structures and implement pass2 of a two pass assembler for pseudo-machine. (BE READY WITH YOUR IC CODE OF PASS 1).

Q3. Design suitable data structures and implement Pass-I of a two-pass macro-processor.

MACRO  
M1 &X, &Y, &A=AREG, &B=  
MOVER &A, &X  
ADD &A, ='1'  
MOVER &B, &Y  
ADD &B, ='5'  
MEND  
  
MACRO  
M2 &P, &Q, &U=CREG, &V=DREG  
MOVER &U, &P  
MOVER &V, &Q  
ADD &U, ='15'  
ADD &V, ='10'  
MEND  
START 100  
M1 10, 20, &B=CREG  
M2 100, 200, &V=AREG, &U=BREG  
END

Q4. Design suitable data structures and implement Pass-II of a two-pass macro-processor.

(BE READY WITH YOUR IC CODE OF PASS 1))

Q5. Write a program to simulate CPU Scheduling Algorithms: FCFS

Q6. Write a program to simulate CPU Scheduling Algorithms: SJF (Preemptive).

Q7. Write a program to simulate CPU Scheduling Algorithms: Priority (Non-Preemptive)

Q8. Write a program to simulate CPU Scheduling Algorithms: Round Robin (Preemptive)

Q9. Write a program to simulate Page replacement algorithm.